REMARKS/ARGUMENTS

Rejection of claim 1-5, 8, 9, and 14 under 35 U.S.C. 102(e) as being anticipated by Nanjo et al (US Patent 6,900,088).

The amended claim 1 of the present invention recites a method for fabricating a semiconductor device, in which the method involves first providing a substrate having at least a first gate structure and a second gate structure thereon. Preferably, both the first gate structure and the second gate structure have sidewalls. A first ion implantation process is then performed to form a shallow-junction doping region of a first conductive type in the substrate next to each sidewall of the first gate structure. After the first ion implantation process is conducted, offset spacers are formed on the sidewalls of the first gate structure and the second gate structure, and after the offset spacers are formed, a second ion implantation process is performed to form a shallow-junction doping region of a second conductive type in the substrate next to the offset spacer on each sidewall of the second gate structure.

Specifically, the first ion implantation process of the claimed invention is performed before the formation of the offset spacers. Applicant asserts that the method disclosed by Nanjo et al does not teach this feature. Inspection of Fig. 6A of the cited reference will reveal that a first gate structure (406a/404a) and a second gate structure (406b/404b) are first disposed on the substrate 401a/401b. Next, as shown in Figs. 6B-6C, a silicon nitride film 409 is formed on the first gate structure and the second gate structure and an etching process is performed to form a spacer 409a/409b around each of the gate structures. Next, as shown in Figs. 6D-6E, the patterned photoresists R41/R43 are used as a mask to perform an ion implantation process to form a source / drain region 410a/410b in the substrate surrounding the first gate structure and the second gate structure. Thereafter, as shown in Figs. 6F-6H, the spacers surrounding the first gate structure and the second gate structure are removed and another ion implantation process

is conducted to form a lightly doped drain 411a/411b in the substrate surrounding the gate structures.

In contrast to the claimed invention of conducting the first ion implantation before the formation of the offset spacers, the first ion implantation process disclosed by Nanjo et al is conducted after the formation of the spacers, as shown in Figs. 6C-6D. In other words, if the cited reference were to reveal the key feature of the claimed invention, the first ion implantation process would be performed as soon as the gate structures 406a/404a/406b/404b are formed and before the spacers are formed.

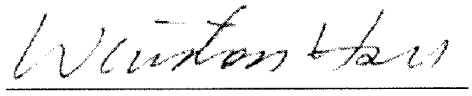
Additionally, the first ion implantation process of the claimed invention specifically forms a shallow-junction doping region of a first conductive type in the substrate next to the sidewall of the first gate structure, and the second ion implantation process specifically forms a shallow-junction doping region of a second conductive type in the substrate next to the sidewall of the offset spacer of the second gate structure. Applicant asserts that these features are both absent in the cited reference. For instance, inspection of Fig. 6D of the cited reference will reveal that the first ion implantation process disclosed by Nanjo et al specifically forms a doping region in the substrate next to the spacer surrounding the first gate structure, but does not form a shallow-junction doping region in the substrate next to the sidewall of the first gate structure. Moreover, Fig. 6E of the cited reference reveals that the second ion implantation process preferably forms a doping region in the substrate next to the spacer surrounding the second gate structure, but does not form a shallow-junction doping region in the substrate next to the offset spacer surrounding the second gate structure.

Since the feature of performing the first ion implantation process before the formation of offset spacers is absent in the cited reference and the location of doping regions formed by the first and second ion implantation is significantly different from the

claimed invention, applicant asserts that Nanjo et al do not teach the method as per the limitation disclosed in amended claim 1 of the present invention. Reconsideration of the amended claim 1 is respectfully requested. As claims 2-5, 8, 9, and 14 are depended upon the amended claim 1, applicant asserts that if amended claim 1 is found allowable, claims 2-5, 8, 9, and 14 should additionally be found allowable. Reconsideration of claims 2-5, 8, 9, and 14 is politely requested.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,



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